**In the Specification:**

Please amend paragraph [0014] of the specification as follows:

**[0014]** FIGS. ~~1a-1i~~ 1a-1j are cross-section views of a wafer after various process steps in accordance with one embodiment of the present invention.

Please amend paragraph [0025] of the specification as follows:

**[0025]** As illustrated in FIG. 1e, the portion of the first dielectric layer 126 (FIG. 1d) located under the notched-spacer masks 130 is removed due to the isotropic etch process, thereby creating [[a]] notched spacers 132. The width of the notch will be dependent upon the thickness of the first dielectric layer 126 and the notch height may be controlled by varying the etch duration. Furthermore, FIG. 1e illustrates the situation in which the first dielectric layer 126 is removed completely to the gate electrode 122. In other situations, a portion of the first dielectric layer 126 may remain on the side of the gate electrode 122, such that the notched spacer is thinner along the surface of the substrate, as illustrated in FIG. 1j. This may be desirable, for example, when it is preferred to control the depth and angle of the implant or to protect the gate electrode 122 or gate dielectric 120 from damage during the etching process or other processes.